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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,234	03/31/2004	David Charles Boutcher	ROC920030387US1	8124

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EXAMINER	
SCHLIE, PAUL W	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 04/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/815,234	BOUTCHER ET AL.	
	Examiner	Art Unit	
	Paul W. Schlie	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-17 have been examined.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-17 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. As elements critical or essential to the practice of the invention are neither included in the claims nor sufficiently enabled by the disclosure in such a way as to enable one skilled in the art to which it pertains, or most nearly related, to make and/or use the invention. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

More specifically, as the disclosure clearly acknowledges (page 8) virtual/logical addressing mechanisms are well known (which one of ordinary skill in the art at the time of the claimed invention understands are utilized to form and transliterate arbitrary virtual/logical addresses into physical ones by maintaining and utilizing translation tables associated with a potential plurality of associated processors and/or processes each potentially restricted to some logically and/or physically addressable sub-regions and having differing logical and/or physical address extents), in view that the disclosed invention claims a method and apparatus apparently performing the same (inclusive of that inherently required by DMA and/or I/O device driver processes) with out any detail disclosed to otherwise indicate the how that claimed is distinguishable from that well

known in the art as inherently utilized by all such systems, in further view that a set of all possible 32-bit logical addresses inherently comprise a subset of all possible 64-bit addresses without the need of any virtual/logical transliteration between the two; it is presumed that some corresponding critical elements necessary to make, use, and/or differentiate the claimed invention must be absent from the disclosure. Corrective action is required, however the applicant is reminded that no mater not supported by the original disclosure may be added.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herrell et al. (5,301,287).

As per independent claims 1, 5 and 12, Herrell et al. teaches that a individual virtual/logical addresses associated with arbitrary process address spaces (partitions) may be either utilized directly by a DMA mechanism as may be desired to transfer data between said potentially distinct address spaces and/or inherently may indicate a particular desired and/or pending such transfer by direct and/or indirect indication (tag) of a data structure comprising the information representing such a buffer and/or corresponding transfer request between multiple logical entities and/or partitions (see abstract lines 8-13 and figure 3); where although Herrell et al. does not explicitly teach

that a supervisory process as may be desired to centrally manage such logical address and/or indication (tag) transliteration may be called a "partition manager", and/or that said logical addresses and/or indications (tags) may be of differing extents (sizes) and require corresponding appropriate interpretation, such choices are considered obvious design choices to one of ordinary skill in the art and typically inherent within the context of a particular system configuration being influenced by factors beyond the scope of the claimed invention; it is considered obvious to combine that taught by Herrell et al. with that considered obvious to one of ordinary skill in the art, for the benefit of enabling the utilization of addresses which may contain sub-ranges which may logically denote particular regions of memory having smaller extents managed by a software process called a "partition manager".

As per claims 2-4, 6-11 and 13-17, being dependent on claims 1, 5, 12, or correspondingly dependent claim inclusively; as Herrell et al. is considered to teach that logical addresses and/or indications (tags) may be utilized to represent buffers (memory regions) communicated between processes and corresponding methods as reviewed above, in view that it is correspondingly well understood by those of ordinary skill in the art that virtual/logical address ranges may be correspondingly mapped in common to arbitrary real (physical) memory and/or otherwise arbitrary logical entities by either a physical apparatus (for example DMA processor) and/or software process (for example device driver), it is considered inherently taught that a predetermined virtual/logical address range may be utilized to denote any corresponding region of real (physical) memory and/or logical entities and utilized for any correspondingly logically consistent

purpose known to those of ordinary skill in the art as per claims (2-4); where as claims (6-11 and 13-17) are considered to encompass claims (2-4) in other form, they are correspondingly rejected based on the same arguments above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul W. Schlie whose telephone number is 571-272-6765. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PIERRE BATAILLE
PRIMARY EXAMINER
4/7/06